CDA 4205 Computer Architecture

Processor Components Implementation II

1. **Objectives**

Using the Logisim Simulator to design the main data path components: a 32 x 32 bit register file and a 4GB byte-addressable memory (1 word = 4 bytes).

1. **Tasks**
2. Model the designed 32x32-bit register file as one single module in Logisim and test the register file for correct operation by writing to and reading from different register combinations.
3. Design and model a 4GB byte-addressable memory system, then test this memory system can read and write a byte, a half word and a word.
4. **Components Design Specifications**
5. **32 x 32 bit Register File**

The register file consists of 32 x 32-bit registers and has the following interface:

Register File

RA

RB

BusA

RegWrite

BusB

RW

5

5

5

32

32

32

BusW

Clock

32

5

5

32

5

32

* 1. BusA and BusB: 32-bit data output busses for reading 2 registers. During read operation, the register file behaves as a combinational block and once the RA or RB have valid data, the content of the read register will appear on BusA or BusB after a certain access time.
  2. RegWrite: control signal to enable/disable register writing operation. When RegWrite is 1, register write is enabled; otherwise, is disabled.
  3. BusW: 32-bit data input bus for writing a register when RegWrite is 1
  4. RA: 5-bits selection lines to select the register to be read on BusA.
  5. RB: 5-bits selection lines to select the register to be read on BusB
  6. RW: 5-bits selection lines to select the register to be to be written with BusW.

1. **4GB byte-addressable memory**

Using the memory modules provided by Logisim to design a 4GB byte-addressable memory. You need to build a memory bank with 4 byte-addressable memory chips and use the address bits A1A0 to enable the selected 1, 2 or 4 memory chips according to byte, half word and word memory reading or writing operations, respectively.